Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. – 6. (Canceled).

7. (Currently Amended) A synchronous data transmission system comprising a first terminal and a second ~~terminals~~ terminal and a synchronous transmission line connected between the first and [[a]] second terminals for voice or image communication with each other, each terminal including a voice or image input means, a sampling clock generator, an A/D converter for digitalizing the output of the voice input means, a data generator, operable with the output of the sampling clock generator, for generating data on the basis of the output of the A/D converter, a transmission buffer receiving the generated data, a plurality of reception buffer stages supplied with the received data via [[a]] an asynchronous transmission line, a data reproducer operable with the output of the sampling clock generator, for reproducing data from the plurality of reception buffer stages, a D/A converter for converting the reproduced data to an analog signal, a voice or image output means for outputting voice based on the D/A converter output, the data stored in the transmission buffer having been packeted in certain time units (t) and being outputted via asynchronous transmission line interface to the asynchronous transmission line for the time unit (t), the data received from the asynchronous transmission line being stored via the asynchronous transmission line interface in the reception buffer, the data stored in the reception buffer being transmitted to the data reproducer, the reception buffer being capable of storing data received from the asynchronous transmission line for a plurality of times (n×t) in every unit time (t), and the data reproducer reproducing data when data for the plurality of times (n×t) has been stored.

8. (Original) The synchronous data transmission system according to claim 7, further comprising a sampling clock synchronizing means for synchronizing the sampling clocks of the sampling clock generators in the first and second terminals by inputting the

output of the sampling clock generator in one terminal to the sampling clock generator in another terminal.

9. (Original) The synchronous data transmission system according to claim 7, wherein the frequency difference between the sampling clocks generated in the sampling clock generators in the first and second terminals is eliminated by inputting the clock from the sampling clock generator in one terminal to the sampling clock generator in another terminal.

10. (Previously Presented) The synchronous data transmission system according to claim 7, wherein the sampling clock frequency of one terminal is made closer to the sampling clock frequency of another terminal by estimating the sampling clock on the basis of the data received directly from the asynchronous transmission line without having been processed in any manner by the one terminal.

11. – 15. (Canceled).

16. (Previously Presented) The synchronous data transmission system according to claim 7, wherein the plurality of reception buffer stages are configured to handle both data underflow and data overflow, without loss of data, due to different sampling clock rates output by the respective sampling clock generator provided in the first and second terminals.

17. (Canceled).

18. (Canceled).